WF4463C

HIGH-PERFORMANCE, LOW-CURRENT TRANSCEIVER

Features

- Frequency range = 142–1050 MHz
- Receive sensitivity = –129 dBm
- Modulation(G)FSK, 4(G)FSK, (G)MSK OOK
- Max output power +20 dBm
- PA support for +27 or +30 dBm
- Low active power consumption
  - 10/13 mA RX
  - 18 mA TX at +10 dBm
- Low current powerdown modes
  - 30 nA shutdown, 40 nA standby
- Preamble sense mode
  - 6 mA average RX current at 1.2 kbps
  - 10 µA average RX current at
- Fast preamble detection
  - 1 byte preamble detection
- Data rate = 100 bps to 1 Mbps
- Power supply = 1.8 to 3.8 V
- Excellent selectivity performance
  - 69 dB adjacent channel
  - 79 dB blocking at 1 MHz
- Antenna diversity and T/R switch control
- Highly configurable packet handler
- TX and RX 64 byte FIFOs
  - 129 bytes dedicated Tx or Rx
- Auto frequency control (AFC)
- Automatic gain control (AGC)
- Low BOM
- Low battery detector
- Temperature sensor
- 20-Pin QFN package
- IEEE 802.15.4g and WMBus compliant
- Suitable for FCC Part 90 Mask D, FCC part 15.247, 15,231, 15,249, ARIB T-108, T-96, T-67, RCR STD-30, China regulatory
- ETSI Category I Operation EN300 220

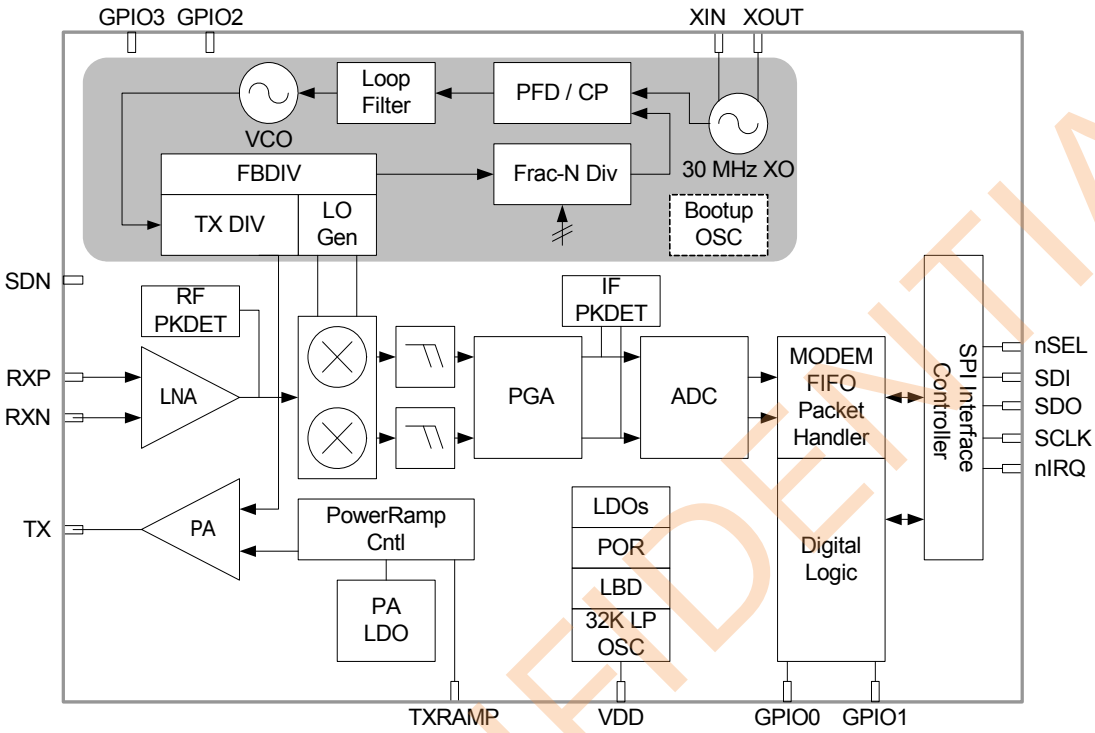
Applications

- Smart metering (802.15.4g and WMBus)
- Remote control
- Home security and alarm
- Telemetry
- Garage and gate openers
- Remote keyless entry
- Home automation
- Industrial control
- Sensor networks
- Health monitors
- Electronic shelf labels

Description

WF4463C is high-performance, low-current transceivers covering the sub-GHz frequency bands from 142 to 1050 MHz. Which includes a complete line of transmitters, receivers, and transceivers covering a wide range of applications. It offer outstanding sensitivity of – 129 dBm while achieving extremely low active and standby current consumption. It offers frequency coverage in all major bands. The WF4463C includes optimal phase noise, blocking, and selectivity performance for narrow band and wireless MBus licensed band applications, such as FCC Part90 and 169 MHz wireless Mbus. The 69 dB adjacent channel selectivity with 12.5 kHz channel spacing ensures robust receive operation in harsh RF conditions, which is particularly important for narrow band operation. The WF4463C offers exceptional output power of up to +20 dBm with outstanding TX efficiency. The high output power and sensitivity results in an industry-leading link budget of 146 dB allowing extended ranges and highly robust communication links. The device can meet worldwide regulatory standards: FCC, ETSI, wireless MBus, and ARIB. All devices are designed to be compliant with 802.15.4g and WMbus smart metering standards.

Functional Block Diagram



1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage Range	V_{DD}		1.8	3.3	3.8	V
Power Saving Modes	$I_{Shutdown}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF	—	30	1300	nA
	$I_{Standby}$	Register values maintained and RC oscillator/WUT OFF	—	40	2900	nA
	$I_{SleepRC}$	RC Oscillator/WUT ON and all register values maintained, and all other blocks OFF	—	740	3800	nA
	$I_{SleepXO}$	Sleep current using an external 32 kHz crystal	—	1.7	—	µA
	$I_{Sensor-LBD}$	Low battery detector ON, register values maintained, and all other blocks OFF	—	1	—	µA
	I_{Ready}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF	—	1.8	—	mA
Preamble Sense Mode Current	I_{psm}	Duty cycling during preamble search, 1.2 kbps, 4 byte preamble	—	6	—	mA
	I_{psm}	Fixed 1 s wakeup interval, 50 kbps, 5 byte preamble	—	10	—	µA
TUNE Mode Current	I_{Tune_RX}	RX Tune, High Performance Mode	—	7.6	—	mA
	I_{Tune_TX}	TX Tune, High Performance Mode	—	7.8	—	mA
RX Mode Current	I_{RXH}	High Performance Mode (measured at 915 MHz and 40 kbps data rate)	—	13.7	22	mA
	I_{RXL}	Low Power Mode (measured at 315 MHz and 40 kbps data rate)	—	10.9	—	mA
TX Mode Current	I_{TX_+20}	+20 dBm output power, Class-E match, 915 MHz, 3.3 V	—	88	108	mA
		+20 dBm output power, square-wave match, 169 MHz, 3.3 V	—	68.5	80	mA
		+13 dBm output power, Class-E match, 915 MHz, 3.3 V	—	44.5	60	mA

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. Measured on direct-tie RF evaluation board.

Table 2. Synthesizer AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Synthesizer Frequency Range	F_{SYN}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
Synthesizer Frequency Resolution	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Synthesizer Settling Time	t_{LOCK}	Measured from exiting Ready mode with XOSC running to any frequency. Including VCO Calibration.	—	50	—	µs
Phase Noise	$L\phi(f_M)$	ΔF = 10 kHz, 169 MHz, High Perf Mode	—	–117	–108	dBc/Hz
		ΔF = 100 kHz, 169 MHz, High Perf Mode	—	–120	–115	dBc/Hz
		ΔF = 1 MHz, 169 MHz, High Perf Mode	—	–138	–135	dBc/Hz
		ΔF = 10 MHz, 169 MHz, High Perf Mode	—	–148	–143	dBc/Hz
		ΔF = 10 kHz, 915 MHz, High Perf Mode	—	–102	–94	dBc/Hz
		ΔF = 100 kHz, 915 MHz, High Perf Mode	—	–105	–97	dBc/Hz
		ΔF = 1 MHz, 915 MHz, High Perf Mode	—	–125	–122	dBc/Hz
		ΔF = 10 MHz, 915 MHz, High Perf Mode	—	–138	–135	dBc/Hz

Note: All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.

Table 3. Receiver AC Electrical Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Frequency Range	F_{RX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
RX Sensitivity 169 MHz[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)	—	–129	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–110	–108	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–106	–104	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–98	–96	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–110	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–89	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–110	–107	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–103	–100	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–97	–93	dBm

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 3. Receiver AC Electrical Characteristics[1,2] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX Sensitivity 915/868 MHz[3]	$P_{RX\_0.5}$	(BER < 0.1%) (500 bps, GFSK, BT = 0.5, Δf = ±250Hz)	—	–127	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)	—	–109	–107	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)	—	–104	–102	dBm
	P_{RX_500}	(BER < 0.1%) (500 kbps, GFSK, BT = 0.5, Δf = ±250 kHz)	—	–97	–92	dBm
	$P_{RX\_9.6}$	(PER 1%) (9.6 kbps, 4GFSK, BT = 0.5, Δf = ±2.4 kHz)	—	–109	—	dBm
	P_{RX_1M}	(PER 1%) (1 Mbps, 4GFSK, BT = 0.5, inner deviation = 83.3 kHz)	—	–88	—	dBm
	P_{RX_OOK}	(BER < 0.1%, 4.8 kbps, 350 kHz BW, OOK, PN15 data)	—	–108	–104	dBm
		(BER < 0.1%, 40 kbps, 350 kHz BW, OOK, PN15 data)	—	–101	–97	dBm
		(BER < 0.1%, 120 kbps, 350 kHz BW, OOK, PN15 data)	—	–96	–91	dBm
RX Channel Bandwidth	BW		1.1	—	850	kHz
RSSI Resolution	RES_{RSSI}	Valid from –110 dBm to –90 dBm	—	±0.5	—	dB
±1-Ch Offset Selectivity, 169 MHz[3]	C/I_{1-CH}	Desired Ref Signal 3 dB above sensitivity, BER < 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz, channel spacing = 12.5 kHz	—	–69	–59	dB
±1-Ch Offset Selectivity, 450 MHz[3]	C/I_{1-CH}		—	–60	–50	dB
±1-Ch Offset Selectivity, 868 / 915 MHz[3]	C/I_{1-CH}		—	–55	–45	dB
Blocking 1 MHz Offset	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity, BER = 0.1%. Interferer is CW, and desired is modulated with 2.4 kbps, ΔF = 1.2 kHz GFSK with BT = 0.5, RX channel BW = 4.8 kHz	—	–79	–68	dB
Blocking 8 MHz Offset	$8M_{BLOCK}$		—	–86	–75	dB

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 3. Receiver AC Electrical Characteristics[1,2] (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Image Rejection (IF = 468.75 kHz)	Im_{REJ}	No image rejection calibration. Rejection at the image frequency. RF = 460 MHz	30	40	—	dB
		With image rejection calibration . Rejection at the image frequency. RF = 460 MHz	40	55	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 915 MHz	30	45	—	dB
		With image rejection calibration. R ejection at the image frequency. RF = 915 MHz	40	52	—	dB
		No image rejection calibration. Rejection at the image frequency. RF = 169 MHz	35	45	—	dB
		With image rejection calibration in . Rejection at the image frequency. RF = 169 MHz	45	60	—	dB

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at V_{DD} = 3.3 V and 25 °C unless otherwise stated.
2. For PER tests, 48 preamble symbols, 4 byte sync word, 10 byte payload and CRC-32 was used.
3. Measured over 50000 bits using PN9 data sequence and data and clock on GPIOs. Sensitivity is expected to be better if reading data from packet handler FIFO especially at higher data rates.

Table 4. Transmitter AC Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX Frequency Range	F_{TX}		850	—	1050	MHz
			350	—	525	MHz
			284	—	350	MHz
			142	—	175	MHz
(G)FSK Data Rate	DR_{FSK}		0.1	—	500	kbps
4(G)FSK Data Rate	DR_{4FSK}		0.2	—	1000	kbps
OOK Data Rate	DR_{OOK}		0.1	—	120	kbps
Modulation Deviation Range	Δf_{960}	850–1050 MHz	—	1.5	—	MHz
	Δf_{525}	420–525 MHz	—	750	—	kHz
	Δf_{420}	350–420 MHz	—	600	—	kHz
	Δf_{350}	283–350 MHz	—	500	—	kHz
	Δf_{175}	142–175 MHz	—	250	—	kHz
Modulation Deviation Resolution	$F_{RES-960}$	850–1050 MHz	—	28.6	—	Hz
	$F_{RES-525}$	420–525 MHz	—	14.3	—	Hz
	$F_{RES-420}$	350–420 MHz	—	11.4	—	Hz
	$F_{RES-350}$	283–350 MHz	—	9.5	—	Hz
	$F_{RES-175}$	142–175 MHz	—	4.7	—	Hz
Output Power Range	P_{TX}	Typical range at 3.3 V with Class E Match optimized for best PA efficiency	–20	—	+20	dBm

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 4. Transmitter AC Electrical Characteristics (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Power Variation		At 20 dBm PA power setting, 915 MHz, Class E match, 3.3 V, 25 °C	19	20	21	dBm
Output Power Variation		At 20 dBm PA power setting, 169 MHz, Square Wave match, 3.3 V, 25 °C	18.5	20	21	dBm
TX RF Output Steps	ΔP_{RF_OUT}	Using switched current match within 6 dB of max power	—	0.25	0.4	dB
TX RF Output Level Variation vs. Temperature	ΔP_{RF_TEMP}	–40 to +85 °C	—	2.3	3	dB
TX RF Output Level Variation vs. Frequency	ΔP_{RF_FREQ}	Measured across 902–928 MHz	—	0.6	1.7	dB
Transmit Modulation Filtering	BT	Gaussian Filtering Bandwith Time Product	—	0.5	—	

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. The maximum data rate is dependent on the XTAL frequency and is calculated as per the formula: Maximum Symbol Rate = Fxtal/60, where Fxtal is the XTAL frequency (typically 30 MHz).
3. Default API setting for modulation deviation resolution is double the typical value specified.
4. Output power is dependent on matching components and board layout.

Table 6. Digital IO Specifications (GPIO_x, SCLK, SDO, SDI, nSEL, nIRQ, SDN)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise Time[2,3]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2.3	—	ns
Fall Time[3,4]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = LL	—	2	—	ns
Input Capacitance	C_{IN}		—	2	—	pF
Logic High Level Input Voltage	V_{IH}		V_{DD} x 0.7	—	—	V
Logic Low Level Input Voltage	V_{IL}		—	—	V_{DD} x 0.3	V
Input Current	I_{IN}	0<V_{IN}< V_{DD}	–1	—	1	µA
Input Current If Pullup is Activated	I_{INP}	V_{IL} = 0 V	1	—	4	µA
Drive Strength for Output Low Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	6.66	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	5.03	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	3.16	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	1.13	—	mA
Drive Strength for Output High Level	I_{OmaxLL}	DRV[1:0] = LL[3]	—	5.75	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	4.37	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	2.73	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.96	—	mA
Drive Strength for Output High Level for GPIO0	I_{OmaxLL}	DRV[1:0] = LL[3]	—	2.53	—	mA
	I_{OmaxLH}	DRV[1:0] = LH[3]	—	2.21	—	mA
	I_{OmaxHL}	DRV[1:0] = HL[3]	—	1.70	—	mA
	I_{OmaxHH}	DRV[1:0] = HH[3]	—	0.80	—	mA
Logic High Level Output Voltage	V_{OH}	DRV[1:0] = HL	V_{DD} x 0.8	—	—	V
Logic Low Level Output Voltage	V_{OL}	DRV[1:0] = HL	—	—	V_{DD} x 0.2	V

Notes:

1. All minimum and maximum values are guaranteed across the recommended operating conditions of supply voltage and from –40 to +85 °C unless otherwise stated. All typical values apply at VDD = 3.3 V and 25 °C unless otherwise stated.
2. 6.7 ns is typical for GPIO0 rise time.
3. Assuming VDD = 3.3 V, drive strength is specified at Voh (min) = 2.64 V and Vol(max) = 0.66 V at room temperature.
4. 2.4 ns is typical for GPIO0 fall time.

Table 7. Thermal Characteristics

Parameter	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Thermal Impedance Junction to Ambient*	θ_{JA}	25	°C/w
Junction Temperature Maximum Value*	T_j	+105	°C
Storage Temperature Range	T_{STG}	–55 to +150	°C
***Note:** θ_{JA} and T_j are based on RF evaluation board measurements.			

Table 8. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	–0.3, +3.8	V
Instantaneous $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +8.0	V
Sustained $V_{RF\text{-}peak}$ to GND on TX Output Pin	–0.3, +6.5	V
Voltage on Analog Inputs	–0.7, V_{DD} + 0.3	V
RX Input Power	+10	dBm
Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Power Amplifier may be damaged if switched on without proper load or termination connected. TX matching network design will influence TX $V_{RF\text{-}peak}$ on TX output pin. Caution: ESD sensitive device.		

2. Functional Description

The WF4463C devices are high-performance, low-current, wireless ISM transceivers that cover the sub-GHz bands.The wide operating voltage range of 1.8–3.8 V and low current consumption make the WF4463C an ideal solution for battery powered applications. The WF4463C operates as a time division duplexing (TDD) transceiver where the device alternately transmits and receives data packets. The device uses a single-conversion mixer to down convert the 2/4-level FSK/GFSK or OOK modulated receive signal to a low IF frequency. Following a programmable gain amplifier (PGA) the signal is converted to the digital domain by a high performance ΔΣ ADC allowing filtering,demodulation, slicing, and packet handling to be performed in the built-in DSP increasing the receiver's performance and flexibility versus analog based architectures. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A single high precision local oscillator (LO) is used for both transmit and receive modes since the transmitter and receiver do not operate at the same time. The LO is generated by an integrated VCO and ΔΣ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates from 100 bps to 1 Mbps. The WF4463C operate in the frequency bands of 142–175, 283–350, 350–525, and 850–1050 MHz with a maximum frequency accuracy step size of 28.6 Hz. The transmit FSK data is modulated directly into the ΔΣ data stream and can be shaped by a Gaussian low-pass filter to reduce unwanted spectral content.

The WF4463C contains a power amplifier (PA) that supports output power up to +20 dBm with very high efficiency,consuming only 70 mA at 169 MHz and 85 mA at 915 MHz. The integrated +20 dBm power amplifier can also be used to compensate for the reduced performance of a lower cost, lower performance antenna or antenna with size constraints due to a small form-factor. Competing solutions require large and expensive external PAs to achieve comparable performance. The PA is single-ended to allow for easy antenna matching and low BOM cost. The PA incorporates automatic ramp-up and ramp-down control to reduce unwanted spectral spreading. The WF4463C supports frequency hopping, TX/RX switch control, and antenna diversity switch control to extend the link range and improve performance. Built-in antenna diversity and support for frequency hopping can be used to further extend range and enhance performance. Antenna diversity is completely integrated into the WF4463C and can improve the system link budget by 8–10 dB, resulting in substantial range increases under adverse environmental conditions. A highly configurable packet handler allows for autonomous encoding/decoding of nearly any packet structure. Additional system features, such as an automatic wake-up timer, low battery detector, 64 byte TX/RX FIFOs, and preamble detection, reduce overall current consumption and allows for the use of lower-cost system MCUs. An integrated temperature sensor, power-on-reset (POR), and GPIOs further reduce overall system cost and size. The WF4463C is designed to work with an MCU, crystal, and a few passive components to create a very low-cost system.

The application shown in Figure 1 is designed for a system with a TX/RX direct-tie configuration without the use of a TX/RX switch. Most applications with output power less than 17 dBm will use this configuration. Figure 2 demonstrates an application for +20 dBm using an external T/R-switch.

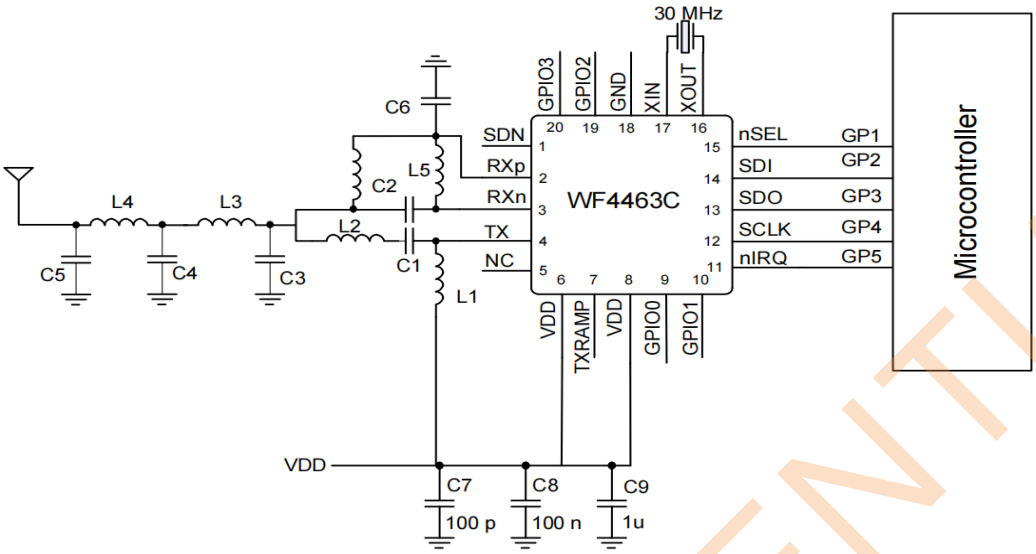


Figure 1. WF4463C Direct Application

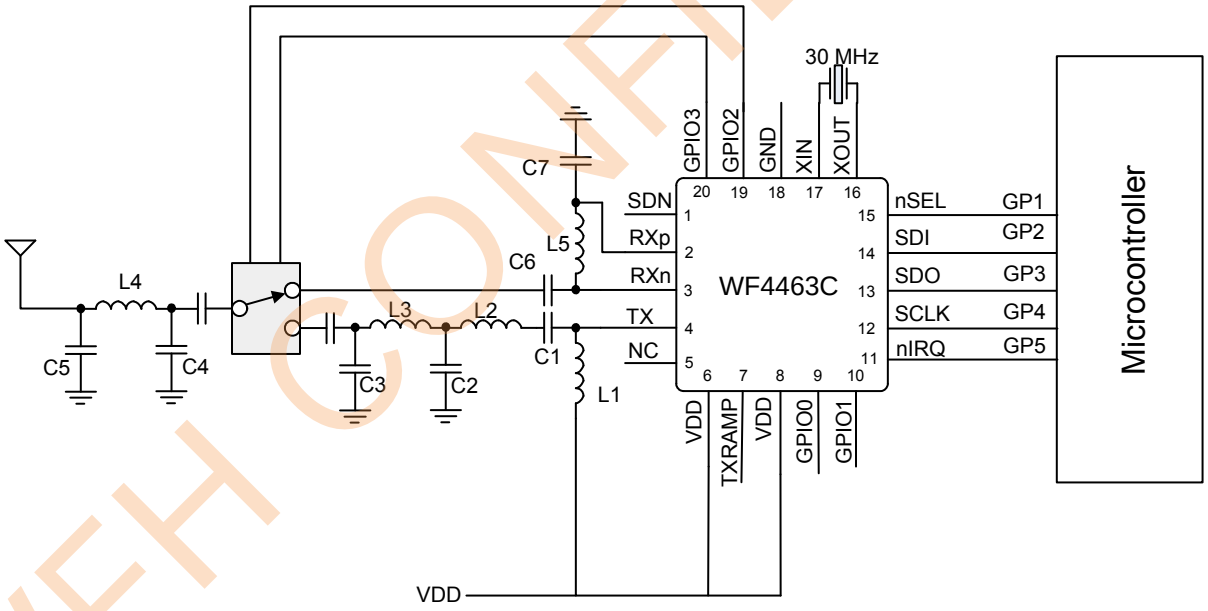


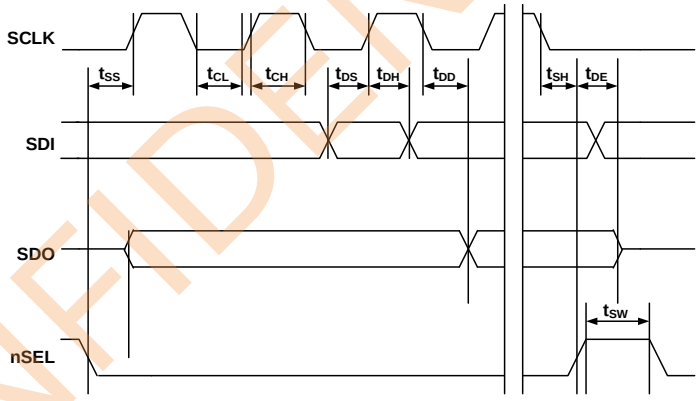
Figure 2. WF4463C Single Antenna with RF Switch

3. Controller Interface

3.1. Serial Peripheral Interface (SPI)

The WF446C communicates with the host MCU over a standard 4-wire serial peripheral interface (SPI): SCLK, SDI,SDO, and nSEL. The SPI interface is designed to operate at a maximum of 10 MHz. The SPI timing parameters are demonstrated in Table 9. The host MCU writes data over the SDI pin and can read data from the device on the SDO output pin. Figure 3 demonstrates an SPI write command. The nSEL pin should go low to initiate the SPI command. The first byte of SDI data will be one of the firmware commands followed by n bytes of parameter data which will be variable depending on the specific command. The rising edges of SCLK should be aligned with the center of the SDI data.

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (ns)	Max (ns)	Diagram
t_{CH}	Clock high time	40		
t_{CL}	Clock low time	40		
t_{DS}	Data setup time	20		
t_{DH}	Data hold time	20		
t_{DD}	Output data delay time		43	
t_{DE}	Output disable time		45	
t_{SS}	Select setup time	20		
t_{SH}	Select hold time	50		
t_{SW}	Select high period	80		

***Note:** CL = 10 pF; VDD = 1.8 V; SDO Drive strength setting = 10.

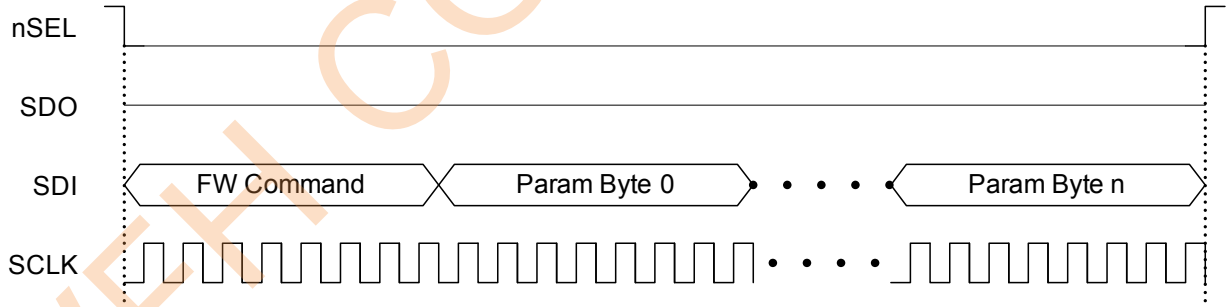
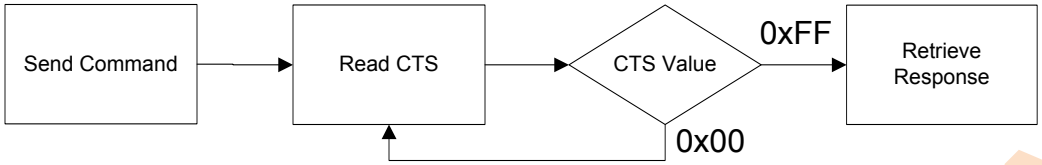


Figure 3. SPI Write Command

The WF4463C contains an internal MCU which controls all the internal functions of the radio. For SPI read commands a typical MCU flow of checking clear-to-send (CTS) is used to make sure the internal MCU has executed the command and prepared the data to be output over the SDO pin. Figure 4 demonstrates the general flow of an SPI read command. Once the CTS value reads FFh then the read data is ready to be clocked out to the host MCU. The typical time for a valid FFh CTS reading is 20 µs. Figure 5 demonstrates the remaining read cycle after CTS is set to FFh. The internal MCU will clock out the SDO data on the negative edge so the host MCU should process the SDO data on the rising edge of SCLK.

Firmware Flow



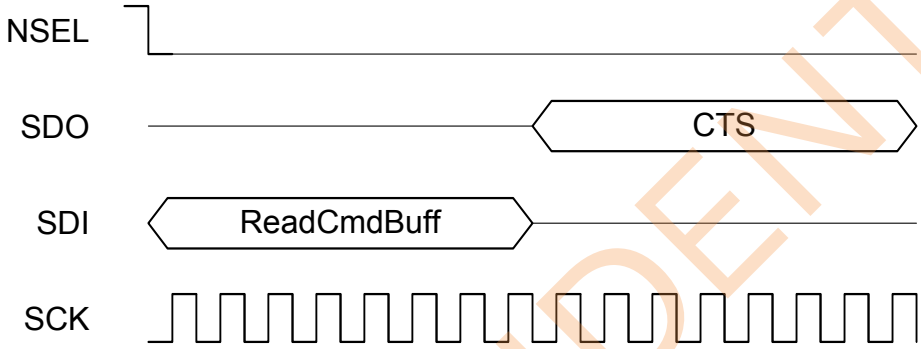


Figure 4. SPI Read Command—Check CTS Value

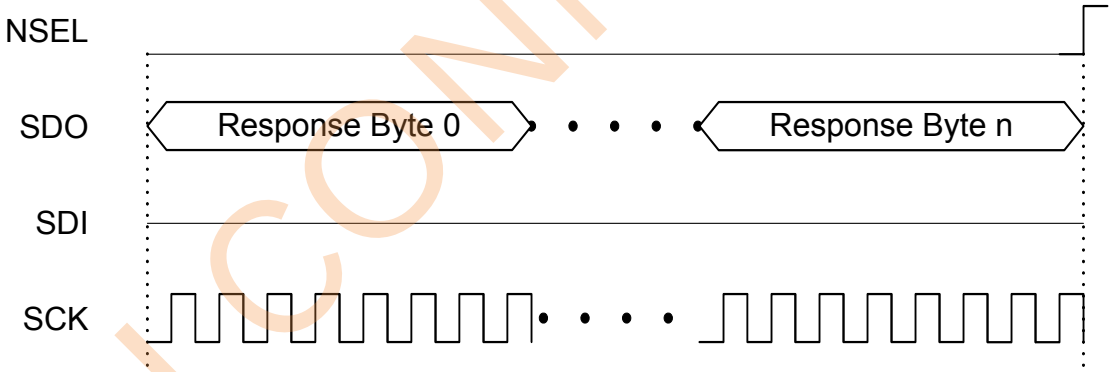
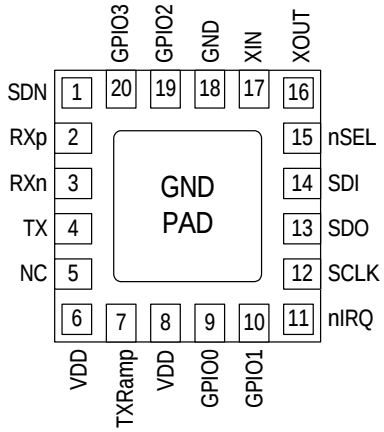


Figure 5. SPI Read Command—Clock Out Read Data

11. Pin Descriptions:



Pin	Pin Name	I/0	Description
1	SDN	I	**Shutdown Input Pin**. 0–VDD V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN = 1, the chip will be completely shut down, and the contents of the registers will be lost.
2	RXp	I	**Differential RF Input Pins of the LNA.** See application schematic for example matching network.
3	RXn	I	
4	TX	O	**Transmit Output Pin.** The PA output is an open-drain connection, so the L-C match must supply VDD (+3.3 VDC nominal) to this pin.
5	NC		It is recommended to connect this pin to GND per the reference design schematic. Not connected internally to any circuitry.
6	VDD	VDD	**+1.8 to +3.8 V Supply Voltage Input to Internal Regulators.** The recommended VDD supply voltage is +3.3 V.
7	TXRAMP	O	**Programmable Bias Output with Ramp Capability for External FET PA.** See "5.4. Transmitter (TX)" on page 33.
8	VDD	VDD	**+1.8 to +3.8 V Supply Voltage Input to Internal Regulators.** The recommended VDD supply voltage is +3.3 V.
9	GPIO0	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
10	GPIO1	I/O	
11	nIRQ	O	**General Microcontroller Interrupt Status Output.** When the WF4463C exhibits any one of the interrupt events, the nIRQ pin will be set low = 0. The Microcontroller can then determine the state of the interrupt by reading the interrupt status. No external resistor pull-up is required, but it may be desirable if multiple interrupt lines are connected.

Pin	Pin Name	I/0	Description
12	SCLK	I	**Serial Clock Input.** 0–VDD V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the WF4463C on positive edge transitions.
13	SDO	O	**0–VDD V Digital Output.** Provides a serial readback function of the internal control registers.
14	SDI	I	**Serial Data Input.** 0–VDD V digital input. This pin provides the serial data stream for the 4-line serial data bus.
15	nSEL	I	**Serial Interface Select Input.** 0–VDD V digital input. This pin provides the Select/Enable function for the 4-line serial data bus.
16	XOUT	O	**Crystal Oscillator Output.** Connect to an external 25 to 32 MHz crystal, or leave floating when driving with an external source on XIN.
17	XIN	I	**Crystal Oscillator Input.** Connect to an external 25 to 32 MHz crystal, or connect to an external source.
18	GND	GND	When using an XTAL, leave floating per the reference design schematic. When using a TCXO, connect to TCXO GND, which should be separate from the board's reference ground plane.
19	GPIO2	I/O	**General Purpose Digital I/O.** May be configured through the registers to perform various functions, including Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, TRSW, AntDiversity control, etc.
20	GPIO3	I/O	
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the WF4463C supplies the RF and cir-cuit ground(s) for the entire chip. It is very important that a good solder con nec-tion is made between this exposed metal paddle and the ground plane of t he PCB underlying the WF4463C.

12. Package Outline:

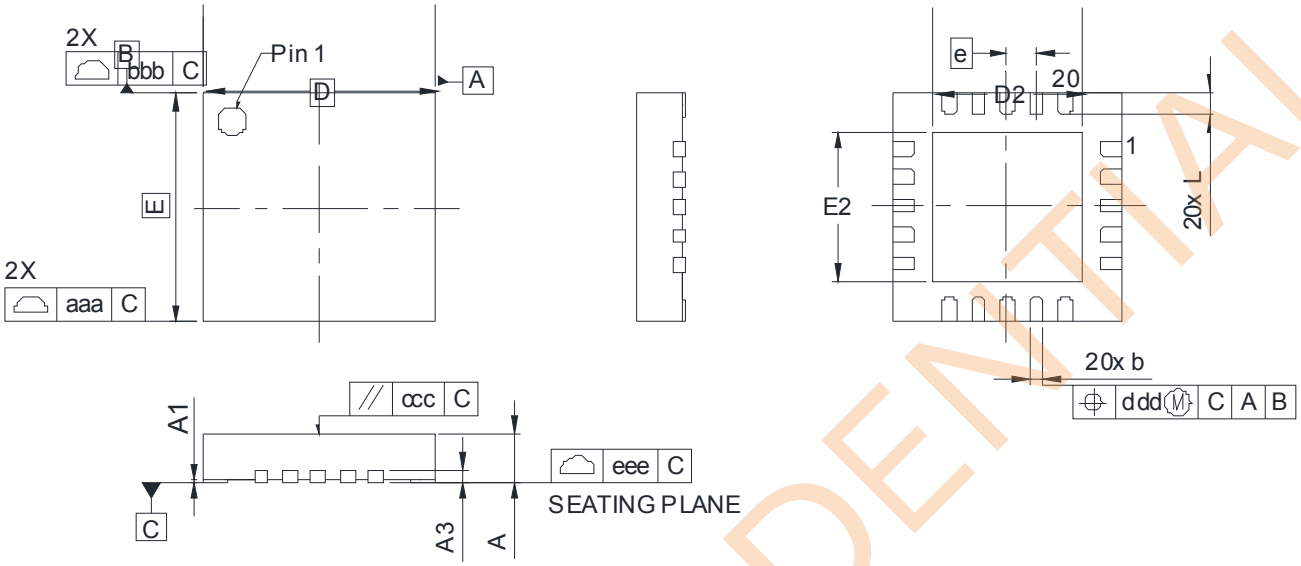


Figure 19. 20-Pin Quad Flat No-Lead (QFN)